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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,209	03/16/2004	Lance Flake	3123-622	3120

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,209	FLAKE, LANCE	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Bauer et al. (USPN 5604753A). As per claims 1,17, Bauer et al. discloses a multi-stage pipeline for fetching or reading information from a memory coupled to the processor, see Figure 6, the pipeline including: a read stage to read a unit of information from the memory in column 11, lines 21-34; a correction stage to correct a soft error detected in a read unit of information in column 6, lines 17-34; a utilization stage to utilized information in the corrected information in column 5, line 55 – column 6, line 16 and column 11, line 35 – column 12, line 6.

3. As per claim 2, Bauer et al. discloses wherein the read stage comprises an instruction read stage to read a program instruction unit of information from the memory in column 11, lines 21-34, wherein the correction stage comprises an instruction correction stage to correct a detected soft error in the read instruction in column 6, lines 17-34; wherein the utilization stage comprises an instruction decode stage to decode the corrected instruction unit of information in column 5, line 55 – column 6, line 16 and column 11, line 35 – column 12, line 6. The decoding is inherent.

4. As per claim 3, Bauer et al. discloses wherein the read stage comprises an instruction read stage to read a program instruction unit of information from the memory in column 11, lines 21-34, wherein the correction stage comprises an instruction correction stage to correct a detected soft error in the read instruction in column 6, lines 17-34; wherein the utilization stage comprises an instruction execution stage to execute the corrected instruction unit of information in column 5, line 55 – column 6, line 16 and column 11, line 35 – column 12, line 6.

5. As per claim 4, Bauer et al. discloses wherein the read stage comprises a data read stage to read a data unit of information from the memory in column 11, lines 21-34, wherein the correction stage comprises a data correction stage to correct a detected soft error in the read data in column 6, lines 17-34, and wherein the decode stage comprises a data decode stage to decode the corrected data unit of information in column 5, line 55 – column 6, line 16 and column 11, line 35 – column 12, line 6.

6. As per claim 5, Bauer et al. discloses wherein the read stage is adapted to read a previously stored unit of information from the memory and an associated error correction code previously stored in the memory in column 11, lines 21-34 and column 5, lines 43-54.

7. As per claim 6, Bauer et al. discloses wherein the previously stored unit of information is 32 bits and the previously stored error correction is a 6 bit Hamming code in column 7, lines 1-15.

8. As per claim 7, Bauer et al. discloses wherein the read stage and the correction stage are both operable within a single cycle of the attached memory in column 9, lines 1-10.

9. As per claim 8, Bauer et al. discloses control logic to enable and disable operation of the correction stage in column 5, lines 43-54.

10. As per claim 9, Bauer et al. discloses correction logic to write the corrected data back to the memory; and notification logic coupled to the correction logic to signal correction the correction logic that corrected data is available in column 5, line 55 – column 6, line 16.

11. As per claim 10, Bauer et al. discloses wherein the notification logic includes error storage for storing the address of the corrected data in the memory in column 5, line 55 – column 6, line 16.

12. As per claim 11, Bauer et al. discloses wherein the error storage further includes error data storage for storing the erroneous value read from the memory in column 5, lines 55-67.

13. As per claim 12, Bauer et al. discloses wherein the multistage pipeline further comprises a write correction stage to write corrected data back to the memory in column 5, line 55 – column 6, line 16.

14. As per claim 13, Bauer et al. discloses wherein the correction logic is implemented as programmed instructions to be executed by the processor in column 7, lines 1-15.

15. As per claim 14, Bauer et al. discloses wherein the notification logic is adapted to generate an interrupt signal in the processor and wherein the correction logic is executed in response to detection of the interrupt signal in column 5, line 55 – column 6, line 16.

16. As per claim 15, Bauer et al. discloses wherein the correction stage is operable within a single cycle of the attached memory in column 9, lines 1-10.

17. As per claim 16, Bauer et al. discloses wherein the correction of a soft error requires more than a single cycle of the attached memory and wherein the pipeline further includes multiple correction stages to correct a soft error detected in a read unit of information in column 5, line 55 – column 6, line 16.

18. As per claim 18, Bauer et al. discloses correcting the read information in multiple correction stages of the processor pipeline in column 5, line 55 – column 6, line 16.

19. As per claim 19, Bauer et al. discloses wherein the steps of correcting and utilizing are performed within a single memory cycle of an attached memory system in column 9, lines 1-10.

20. As per claim 20, Bauer et al. discloses selectively disabling operation of the correction stage in column 5, lines 43-54.

21. As per claim 21, Bauer et al. discloses reading a unit of data; and reading a corresponding error correcting code previously stored with the unit of data in column 11, lines 21-34 and column 5, lines 43-54.

22. As per claim 22, Bauer et al. discloses wherein the step of reading a unit of data comprises reading a 32 bit data value and wherein the step of reading a corresponding error correcting code comprises reading a 6 bit Hamming code in column 7, lines 1-15.

23. As per claim 23, Bauer et al. discloses storing information regarding a soft error corrected in the step of correcting in column 5, line 55 – column 6, line 16.

24. As per claim 24, Bauer et al. discloses saving an address value of the location that provided the corrected soft error in column 5, line 55 – column 6, line 16.

25. As per claim 25, Bauer et al. discloses saving an erroneous data value that provided the corrected soft error in column 5, line 55 – column 6, line 16.

26. As per claim 26, Bauer et al. discloses notifying the processor that a soft error was corrected in column 5, line 55 – column 6, line 16.

27. As per claim 27, Bauer et al. discloses executing instructions in the processor to write the corrected information into the memory in column 5, line 55 – column 6, line 16.

28. As per claim 28, Bauer et al. discloses interrupting the processor to signal correction of a soft error in column 5, line 55 – column 6, line 16.

29. As per claim 29, Bauer et al. discloses writing the corrected information to the memory in a write corrected information stage of the processor pipeline in column 5, line 55 – column 6, line 16.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson
Examiner
Art Unit 2113